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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
I4303.0075	

Application Number	Filed
10/040,727-Conf. #2597	December 28, 2001
First Named Inventor: Stefan J. Bitterlich et al.	
Art Unit: 2611	Examiner: P. M. Phu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant /inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 38,395
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

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May 9, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of 1 forms are submitted.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV262795655US, on the date shown below in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: May 9, 2006 Signature: Laura C. Brutman (Laura C. Brutman)

Docket No.: I4303.0075
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Stefan J. Bitterlich et al.

Application No.: 10/040,727 | Confirmation No.: 2597

Filed: December 28, 2001 | Art Unit: 2611

For: CHANNEL CODEC PROCESSOR CONFIGURABLE FOR MULTIPLE WIRELESS COMMUNICATIONS STANDARDS | Examiner: P. M. Phu

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants respectfully request a review of the legal and factual bases for the rejections in the above-identified patent application. Pursuant to the guidelines set forth in the Official Gazette Notice of July 12, 2005 for the Pre-Appeal Brief Conference Program, favorable reconsideration of the subject application is respectfully requested in view of the following remarks.

According to the Advisory Action dated April 4, 2006, claims 1-37 remain rejected under 35 USC 102(e) as being anticipated by Subramanian et al. (2002/0015401; hereinafter, "Subramanian I"), and also remain rejected under 35 USC 102(e) as being anticipated by Subramanian et al. (2002/0031166) (hereinafter, "Subramanian II").

The present invention is directed to a channel CODEC processor 104 having an algorithm-specific kernel block 212-218, 252-258 and a processor core 210, 250. See Figs. 1 and 2. The algorithm-specific kernel block 212-218, 252-258 is operable to receive a data stream, and includes logic tailored to perform at least one step of a channel CODEC algorithm on the data stream. The processor core is coupled to provide configuration data to the algorithm-specific kernel block, wherein the configuration data causes the kernel block to perform the at least one step of the channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

Both Subramanian I and Subramanian II are assigned to the assignee of the present application, Infineon Technologies AG. Neither of these applied references teaches or even suggests the claimed channel CODEC processor. That is, neither of these references teaches a channel CODEC processor having a processor core that provides an algorithm-specific kernel block with configuration data, as required by the claimed invention.

Before specifically explaining why the applied references do not teach a channel CODEC processor having a processor core, it may be helpful to first identify corresponding figures in the application and the two references (i.e., Subramanian I and Subramanian II). As mentioned above, the application and applied references are all assigned to Infineon Technologies, and as a result the figures have similar layouts. Fig. 1 of the present application shows an electronic communication device, as does Figs. 1B in each of Subramanian I and Subramanian II. Each of these figures includes a configurable channel codec processor 104, and a processor (DSP/μp) 112. Fig. 2 of the present application shows the details of the configurable channel codec processor 104,

which includes the claimed processor core 210, 250; there is no such corresponding figure in either of Subramanian I or Subramanian II.

On pages 12 and 13 of the final Office Action the Examiner specifically states that she believes each of Subramanian I and Subramanian II teaches the claimed processor core of the channel CODEC to be the processor (DSP/μp) 112. This processor 112 is shown in each of the corresponding figures of the present application and Subramanian I and Subramanian II. However, this processor 112 can not be the claimed processor core 210, 250 because it is not located in the channel CODEC processor 104, as required by the claimed invention. Fig. 2 of the present application shows the details of the channel CODEC processor 104, which includes the claimed processor core 210, 250. Subramanian I and Subramanian II do not show such a processor core 210, 250.

Comparing the architectures of block 200 of Figure 2 of the present application and block 100 of Figure 1B in each of the Subramanian references shows that the processor cores 210 and 250 of Figure 2 of the present application connect to other blocks directly for configuration data while they also connect to other blocks via a switchable/reconfigurable interconnect 230 and 270 for all other purposes. Processor 112, which is shown in Figure 1B of the Subramanian references and in Fig. 1 of the present application, directly connects blocks 102a, 102b and 104 for all purposes. Processor 112 connects to other blocks (116, 118, 110a, and 108) via bus 126. since the architectures of the Subramanian references of the claimed invention are different, it should be clear that the processor 112 can not be the claimed processor core 210, 250. The claims are therefore patentable over the applied references for at least this reason.

Contrary to the Examiner's statements on pages 12 and 13 of the final Office Action, Subramanian I and Subramanian II do not disclose an algorithm specific kernel block at 102a and 104. In Subramanian I and Subramanian II, and also in the present

application, reference numeral 102a instead represents a modem processor, and reference numeral 104 represents a channel CODEC processor. (See Fig. 1 of the present application, and Fig. 1B in each of Subramanian I and Subramanian II.) The claimed algorithm specific kernel blocks 212-218, 252-258 are located within the channel CODEC processor 104, as illustrated in Fig. 2 of the present application; again, there is no such corresponding structure or figure in either of Subramanian I and Subramanian II.

Considering the functionality of block 100 of Figure 1B of the Subramanian references and Fig. 1 of the present application, blocks 102a and 102b are an integration of at least one hardware kernel plane including multiple kernel functions to realize complete signal modulation and demodulation function. On the other hand, considering the functionality of block 200 of Fig. 2 of the present application, blocks 212, 214, 216, 218, 252, 254, 256 and 258 are individual kernel functions; only their combination together with processor cores 210 and 250 and memory 202 and 242 results in the realization of complete channel coding and decoding function. Thus, it is clear that functionality of the algorithm specific kernel blocks 212-218, 252-258 is completely different from the functionality of the blocks 102a and 102b.

Thus, for the reasons stated above, Applicant respectfully submits that neither of the references anticipates all of the elements of the presently claimed invention.

Applicants respectfully submit that pending claims 1-37 are allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Dated: May 9, 2006

Respectfully submitted,

By Laura C. Brutman

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